Amendments to the Specification

Please rewrite the Section Heading on page 3, line 6 as follows:

~~DISCLOSURE~~ SUMMARY OF THE INVENTION

Please rewrite the paragraph on page 6, lines 16-17 as follows:

Fig. 1 is an exploded perspective view of a passive component according to a first embodiment[[:]].

Please rewrite the paragraph on page 6, line2 18-19 as follows:

Fig. 2 is a vertical cross-sectional view of the passive component according to the first embodiment[[:]].

Please rewrite the paragraph on page 6, lines 20-21 as follows:

Fig. 3 is an exploded perspective view of a passive component according to a second embodiment[[:]].

Please rewrite the paragraph on page 6, lines 22-23 as follows:

Fig. 4 is a vertical cross-sectional view of the passive component according to the second embodiment[[:]].

Please rewrite the paragraph on page 6, lines 24-25 as follows:

Fig. 5 is an exploded perspective view of a passive component according to a third embodiment[[:]].

Please rewrite the paragraph on page 6, lines 26-27 as follows:

Fig. 6 is a vertical cross-sectional view of the passive component according to the third embodiment[[:]].

Please rewrite the paragraph on page 7, lines 1-2 as follows:

Fig. 7 is an exploded perspective view of a passive component according to a fifth embodiment~~: and~~.

Please rewrite the Section Heading on page 7, line 6 as follows:

~~BEST MODE FOR CARRYING OUT~~ DETAILED DESCRIPTION OF THE INVENTION

Please rewrite the paragraph on page 7, lines 11-18 as follows:

As shown in FIGS. 1 and 2, a passive component 10A according to a first embodiment has a dielectric substrate 14 including a plurality of dielectric layers (S1 ~~through~~ , S2, S3, S4, S5, S6, S7) stacked and sintered together and inner-layer shield electrodes 12a, 12b disposed respectively on ~~both principal surfaces~~ (a principal surface of the second dielectric layer S2 and a principal surface of the sixth dielectric layer S6~~)~~.

Please rewrite the paragraph on page 7, lines 19-23 as follows:

The dielectric substrate 14 is constructed by successively stacking the first through seventh dielectric layers S1 through S7. Each of the first through seventh dielectric layers S1 ~~through~~, S2, S3, S4, S5, S6, S7 ~~comprises~~ comprise a single layer or a plurality of layers.

Please rewrite the paragraph bridging page 9, lines 27 to page 10, line 9 as follows:

The input electrode layer 48 is disposed in the vicinity of the second side surface 14b of the dielectric substrate 14. The output electrode layer 50 is disposed in the vicinity of the third side surface 14c of the dielectric substrate 14. Of the four shield electrode layers 52a ~~through~~, 52b, 52c, 52d, the two shield electrode layers 52a, 52b are disposed in the vicinity of the first side surface 14a of the dielectric substrate 14, and the other two shield electrode layers 52c, 52d are disposed in the vicinity of the fourth side surface 14d of the dielectric substrate 14.

Please rewrite the paragraph on page 10, lines 10-19 as follows:

The input electrode layer 48 is electrically connected to the input resonant electrode 26 through a via hole 54 extending through the fourth through sixth dielectric layers S4 ~~through~~, S5, S6 and the input tap electrode 30 in the second side surface 14b of the dielectric substrate 14. The output electrode layer 50 is electrically connected to the output resonant electrode 28 through a via hole 56 extending through the fourth through sixth dielectric layers S4 ~~through~~, S5, S6 and the output tap electrode 32 in the third side surface 14c of the dielectric substrate 14.

Please rewrite the paragraph bridging page 10, line 27 to page 11, line 3 as follows:

The diameters of the input electrode layer 48, the output electrode layer 50, and the four shield electrode layers 52a ~~through~~, 52b, 52c, 52d are greater than the diameters of the via holes 22, 24, 44, and 46.

Please rewrite the paragraph on page 11, lines 4-12 as follows:

With the passive component 10A according to the first embodiment, as described above, the input electrode layer 48 serving as the input terminal, the output electrode layer 50 serving as the output terminal, and the four shield electrode layers 52a ~~through~~, 52b, 52c, 52d serving as the shield terminals are disposed as via holes in the lowermost dielectric layer S7. Therefore, the input terminal, the output terminal, and the shield terminals are provided only on the lower surface of the dielectric substrate 14.

Please rewrite the paragraph bridging page 12, line 25 to page 13, line 8 as follows:

Particularly, inasmuch as the diameters of the electrode layers 48, 50, 52a ~~through~~, 52b, 52c, 52d are greater than the diameters of the via holes 22, 24, 44, 45, 46, and 47, as shown in FIG. 2, the area in which an input wiring pattern 62 on a wiring board 60 and the input electrode layer 48 face each other, the area in which an output wiring pattern 64 and the output electrode layer 50 face each other, and the area

in which a shield wiring pattern 66 and the shield electrode layers 52a ~~through~~, 52b, 52c, 52d face each other are increased to suppress an unwanted inductive component from forming.

Please rewrite the paragraph on page 13, lines 12-17 as follows:

As shown in FIGS. 3 and 4, the passive component 10B according to the second embodiment is of essentially the same structure as the passive component 10A according to the first embodiment, but differs therefrom in that the input resonator 18 and the output resonator 20 are constructed of via holes 70, 72. Repeat descriptions of like elements are deleted.

Please rewrite the paragraph on page 19, lines 5-15 as follows:

As shown in FIG. 5, the passive component 10C according to the third embodiment is of essentially the same structure as the passive component 10B according to the second embodiment, but differs therefrom in that the shield electrode films 96, 98 (see FIG. 3) are not disposed on the lower surface of the dielectric substrate 14, and, of the dielectric layers S1 ~~through~~, S2, S3, S4, S5, S6, S7 that make up the dielectric substrate 14, the sixth and seventh dielectric layers S6, S7 between the inner-layer shield electrode 12b and the lower surface of the dielectric substrate 14 are made of a material having a dielectric constant εr (> 20). Repeat descriptions of like elements are omitted.

Please rewrite the paragraph bridging page 24, line 21 to page 25, line 8 as follows:

The passive component 10E according to the fifth embodiment has an inner-layer shield electrode 212 disposed on a principal surface of the tenth dielectric layer S10. On the lower surface of the eleventh dielectric layer S11, there are disposed shield terminals 218a ~~through~~, 218b, 218c, 218d respectively in a corner 214 including the first and third side surfaces 14a, 14c of the dielectric substrate 14, a region including a central portion of the first side surface 14a, a corner 216 including the second and fourth side surfaces 14b, 14d, and a region including a central portion of

the fourth side surface 14d, an input terminal 222 in a corner 220 including the third and fourth side surfaces 14c, 14d of the dielectric substrate 14, and an output terminal 226 in a corner 224 including the first and second side surfaces 14a, 14b of the dielectric substrate 14.

Please rewrite the paragraph on page 25, lines 9-14 as follows:

The second through fifth dielectric layers S2 through S5 have, on principal surfaces thereof, first through fifth inductive electrodes 228a ~~through~~, 228b, 228c, 228d, 228e for providing inductance. The first through fifth inductive electrodes 228a through 228e are connected and formed into a coil by via holes 230, 232, 234, 236.

Please rewrite the paragraph on page 25, lines 15-18 as follows:

The seventh through ninth dielectric layers S7 through S9 have, on principal surfaces thereof, first through fourth capacitive electrodes 238a ~~through~~, 238b, 238c, 238d for providing capacitance.

Please rewrite the paragraph on page 27, lines 2-13 as follows:

With the passive component 10E according to the fifth embodiment, of the six terminals 218a through 218d, 222, 226 on the lower surface of the dielectric substrate 14, the input terminal 222 and the output terminal 226 are located diagonally opposite to each other, and the shield terminals 218a through 218d are located in other regions. However, as shown in FIG. 8, if eight terminals (input and output terminals (in/out) 250a ~~through~~, 250b, 250c, 250d, and shield terminals (GND) 252a ~~through~~, 252b, 252c, 252d), for example, are disposed on the lower surface of the dielectric substrate 14, then the input and output terminals 250a ~~through~~, 250b, 250c, 250d and the shield terminals 252a ~~through~~, 252b, 252c, 252d may be arranged in a checkerboard pattern.